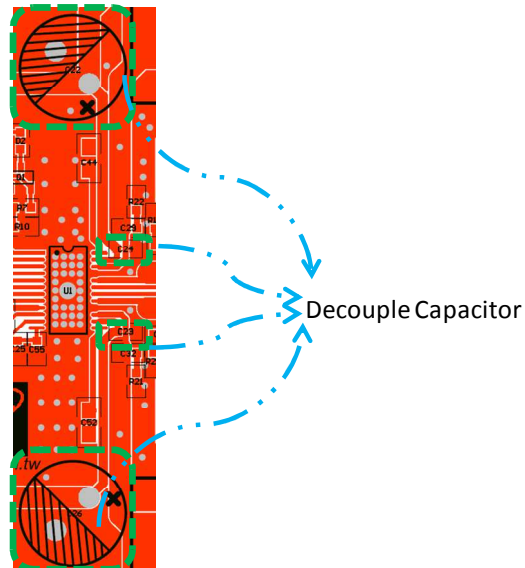


AD82584F (E-TSSOP-24L) Layout Guide

Due to Class-D switching edges are fast, it's necessary to take care when planning the layout of the printed circuit board.

- Large bulk capacitor (470uF) should be placed near the AD82584F on the VDDL and VDDR supplies to avoid power bouncing. The high frequency decoupling capacitors should be placed as close to the VDDL and VDDR terminals as possible. A small and good quality low ESR ceramic capacitor between 220pF and 1000pF and a larger mid frequency cap of value between 0.1uF and 1uF is good quality to VDDL and VDDR also.

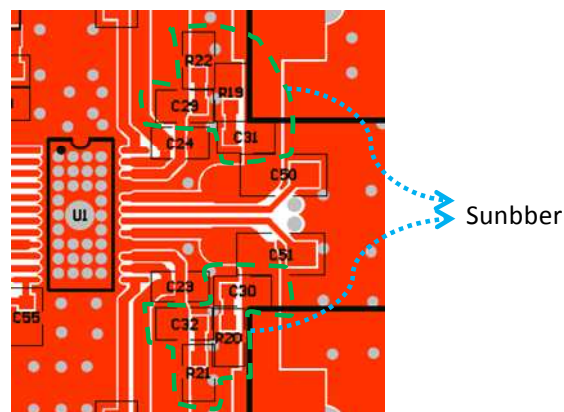
- EMI and Performance considering



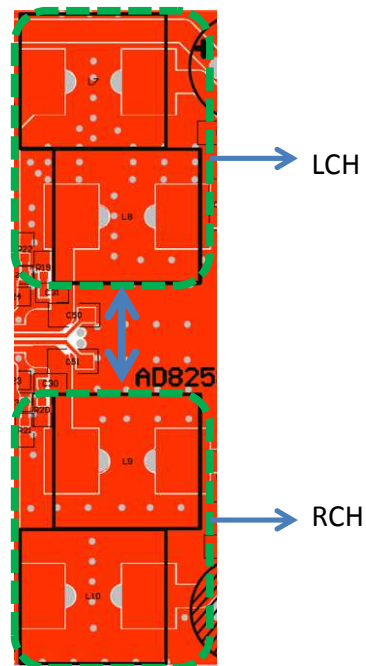
- In order to avoid spike issue of PWM signal, the snubber circuit should be placed as close to the output pin (LA, LB, RA and RB)

Note. Snubber circuit is not necessary if PVDD $\leq$ 20V.

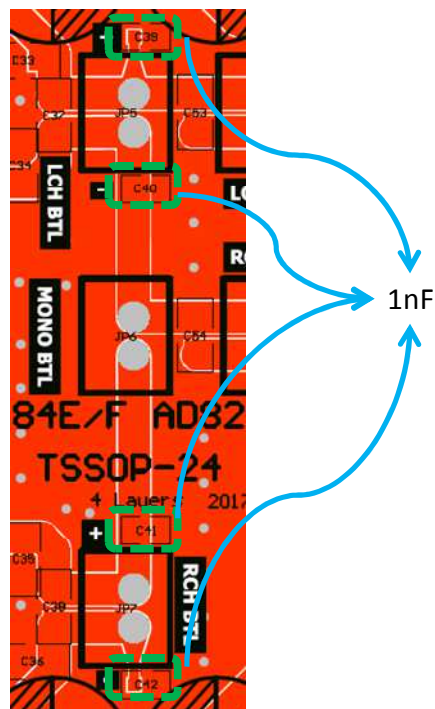
- EMI considering



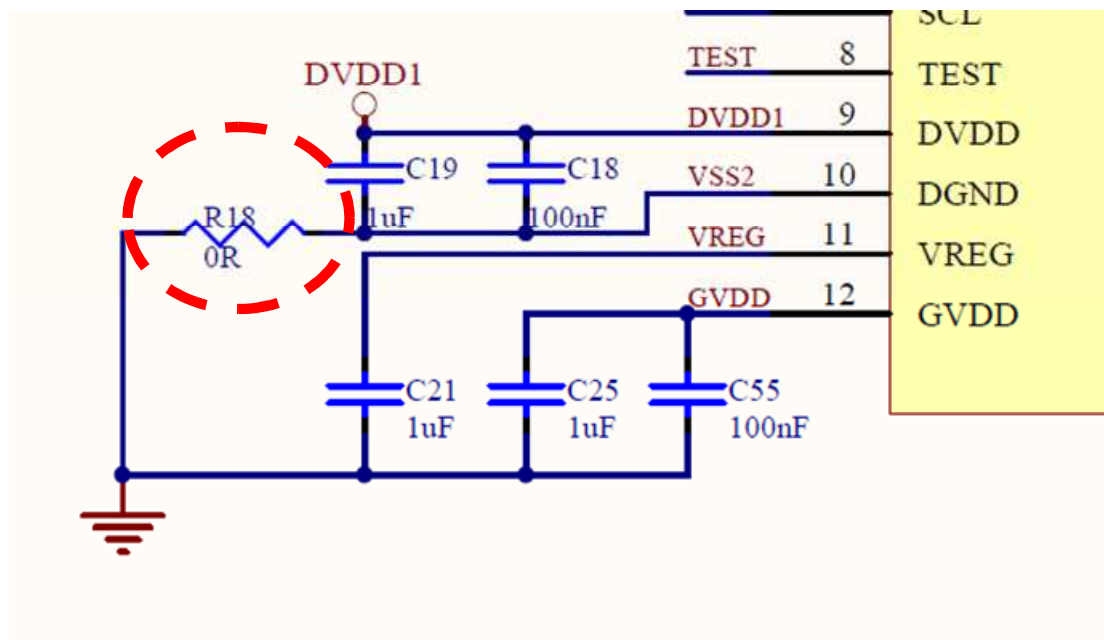
- The inductor is not suggested to put it to close between two channels (L and R channel). It's not need to care this if the shield inductor is adopted.
- Channel separation, cross-talk considering



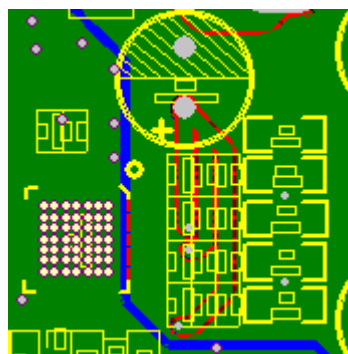
- Output filter circuit, 1nF capacitor should be close to the output terminals as possible for the best EMI performance.
- EMI considering



- In order to avoid OC (Over Current) malfunction, please adding a 0ohm resistance between DGND and GND.



- HV (VDDL/R) power line, please keep the trace width >1mm. Don't keep the power line in alignment (Bulk capacitor to VDDL and then to VDDR). It's better to get good audio performance during high output power by the parallel trace layout between bulk capacitor (470uF) to VDDL/R.



- Thermal pad

The thermal pad must be soldered to the PCB for thermal performance and optimal reliability.

- The dimensions of the thermal land area should be 4.7mm x 2.9mm. 7x3 (21 vias) solid via should be equally spaced underneath the thermal land. The vias must be solid via, not thermal relief or webbed via.
- If 2-layer PCB is adopted, the bottom layer thermal land area large and completed is important for AD82584F chip power dissipation. The poor thermal performance will be suffered if the thermal land area is not large enough on the PCB.
- If 4-layer PCB is adopted, it will have good thermal performance as below suggested.

Top Layer : To keep it for LV and HV signal trace.

MidLayer 1 : To keep it for LV GND and HV GND.

MidLayer 2 : To keep it for LV power line and HV power line.

Bottom Layer : To keep it for LV GND, keep this thermal land area large and completed more.

- PCB recommend pad layout dimension (E-TSSOP-24L)

